transistor device formed as part of a memory cell in the memory device;

selectively etching the resultant structure to a given depth to form trenches;

depositing a second insulating layer over said structure including said trenches;

selectively removing said second insulating layer so as to form element isolation regions composed of the trenches filled with said second insulating layer;

B1 cont.

removing said first insulating layer; and

selectively removing said second insulating layer using a chemical mechanical polishing (CMP) process until a surface of the floating gate conductive layer is substantially even with a surface of the second insulating layer, the floating gate conductive layer being used as a stopping layer for the CMP process.

B2

3. (Amended) A method as defined in Claim 1, wherein said floating gate conductive layer has a thickness of 50 to 1000Å.

B3

7. (Amended) A method as defined in Claim 6, wherein the step of selectively removing said flattened first insulating layer is performed until said floating gate conductive layer is exposed.

B4

9. (Amended) A method as defined in Claim 1, wherein the step of selectively removing said second insulating layer by the CMP process employs a slurry with selectivity between said second insulating layer and the floating gate conductive layer equal to or greater than 1.